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Total No. of Pages : 02

Total No. of Questions : 18

B.Tech. (CSE) / (IT) (2012 to 2017) (Sem.-3)

COMPUTER ARCHITECTURE

Subject Code : BTCS-301

M.Code : 56591

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION-A

Write briefly :

- 1) What do you mean by register transfer language in computer architecture?
- 2) What is an instruction format in computer architecture?
- 3) Discuss array processors.
- 4) Compare RISC with CISC?.
- 5) What are the benefits of virtual memory?
- 6) Discuss timing and control.
- 7) Define Instruction level pipelining.
- 8) What is mapping functions in cache memory?
- 9) Write the benefits of serial communication?
- 10) Discuss memory synchronization.

SECTION-B

- 11) What are the special registers in a typical computer? Explain their purposes in detail.
- 12) What do you understand by interrupt? Explain the steps through which the processor handles the interrupts.
- 13) What are the advantages and disadvantages of hardwired and microprogrammed control?
- 14) What is DMA? Give an example where DMA mode of data transfer is useful?
- 15) What are addressing modes? Explain the various addressing modes with examples.

SECTION-C

- 16) Describe in brief the architecture of a vector processor. What are some of the key limitations of this architecture?
- 17) Write short notes on following :
 - a. Interprocessor communication and synchronization
 - b. Asynchronous data transfer
- 18) Explain various mechanisms of data transfer from a peripheral device.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.